Ordering number : EN5003

CMOS LSI

SANYO

No. 5003

LC66556B, 66558B

Four-Bit Single-Chip Microcontrollers with 6 k and 8 k Bytes of On-Chip ROM

Overview

The LC66556B and LC66558B are four-bit single-chip CMOS microcontrollers that integrate on a single chip all the functions required in a microcontroller, including ROM, RAM, I/O ports, two serial interfaces, comparator inputs, three-value inputs, timers and interrupts. These products are provided in a 64-pin package.

These products differ from the earlier LC66558A Series in the power supply voltage range and certain other electrical characteristics.

Features and Functions

- On-chip ROM and RAM with 6 k (or 8 k) byte and 512 × 4-bit capacities
- The same instruction set (with 127 instructions) as the LC66000 Series (except that the SB instruction is not supported)
- I/O ports: 54 pins
- 8-bit serial interface: two circuits (16-bit cascade connection supported)
- Instruction cycle: 0.92 to 10 μs (at 3 to 5.5 V)
- Powerful timers and prescalers
  12-bit timer: time-limit timer, event counter, pulse width measurement, square wave output
  8-bit timer: time-limit timer, event counter, PWM output, square wave output
  12-bit prescaler: time base functions
- Powerful 11-factor 8-vector interrupt system
  External interrupts: 6 factors/3 vectors
  Internal interrupts: 5 factors/5 vectors
- Flexible I/O functions
  Comparator inputs, three-value inputs, 20 mA drive outputs, 15 V breakdown voltage pins, pull-up/open-drain option switching possible
- Runaway detection function (watchdog timer) option
- 8-bit I/O function
- Power saving functions: halt and hold modes
  Package: DIP64S, QFP64E
- Evaluation LSI: LC66599 (evaluation chip) + EVA850/800-TB665XX
  LC66E516 (On-chip EPROM microcontrollers)
  LC66P516 (On-chip OTPROM microcontrollers)

Series Structure

Type No.	Pin count	ROM capacity	RAM capacity	Package		Features
LC66304A/306A/308A	42	4 k/6 k/8 kB	512 W	DIP42S	QFP48E	Normal versions 4.0 to 6.0 V/0.92 μs
LC66404A/406A/408A	42	4 k/6 k/8 kB	512 W	DIP42S	QFP48E	
LC66506B/508B/512B/516B	64	6 k/8 k/12 k/16 kB	512 W	DIP64S	QFP64A	
LC66354A/356A/358A	42	4 k/6 k/8 kB	512 W	DIP42S	QFP48E	Low-voltage versions 2.2 to 5.5 V/3.92 μs
LC66354S/356S/358S*	42	4 k/6 k/8 kB	512 W		QFP44M	
LC66556A/558A/562A/566A	64	6 k/8 k/12 k/16 kB	512 W	DIP64S	QFP64E	
LC66354B/356B/358B	42	4 k/6 k/8 kB	512 W	DIP42S	QFP48E	Low-voltage high-speed versions 3.0 to 5.5 V/0.92 μs
LC66556B/558B	64	6 k/8 k	512 W	DIP64S	QFP64E	
LC66562B/566B	64	12 k/16 kB	512 W	DIP64S	QFP64E	
LC66E308	42	EPROM 8 kB	512 W	DIC42S (window)	QFC48 (window)	Evaluation (window) versions & OTP versions 4.5 to 5.5 V/0.92 μs
LC66P308	42	OTPROM 8 kB	512 W	DIC42S	QFP48E	
LC66E408	42	EPROM 8 kB	512 W	DIC42S (window)	QFC48 (window)	
LC66P408	42	OTPROM 8 kB	512 W	DIC42S	QFP48E	
LC66E516	64	EPROM 16 kB	512 W	DIC64S (window)	QFC64 (window)	
LC66P516	64	OTPROM 16 kB	512 W	DIC64S	QFP64E	

Note: *: Under development

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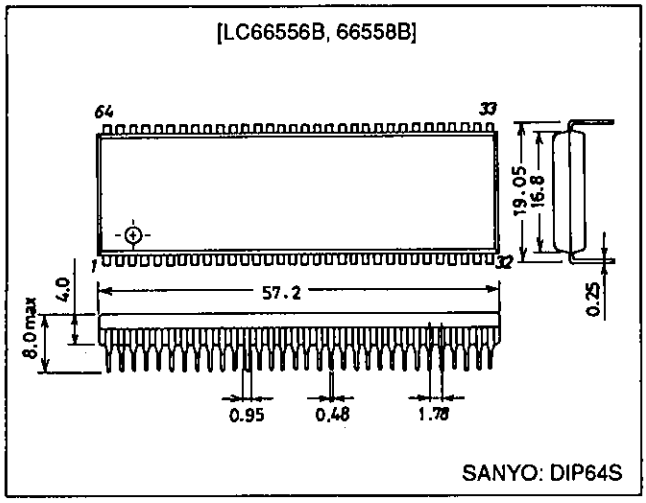
Package Dimensions

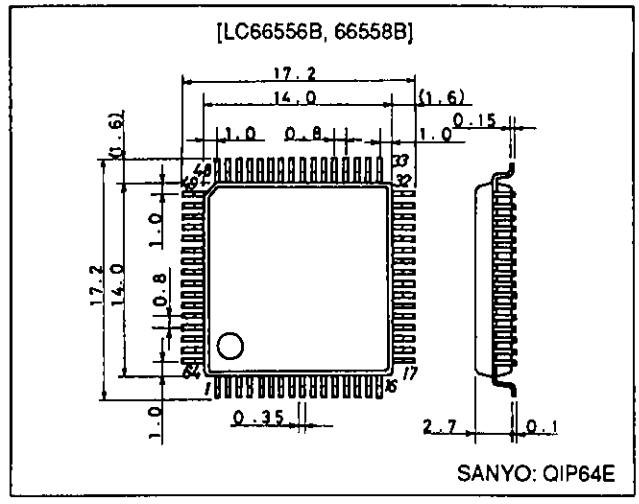
unit: mm

3071-DIP64S

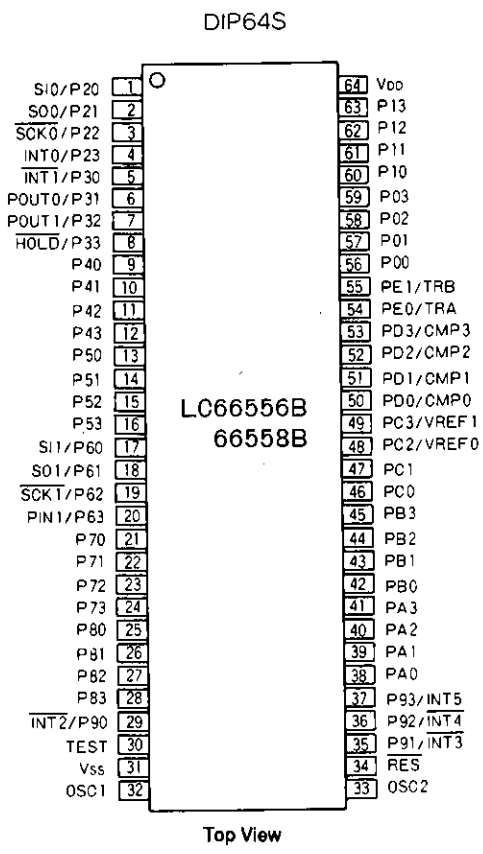


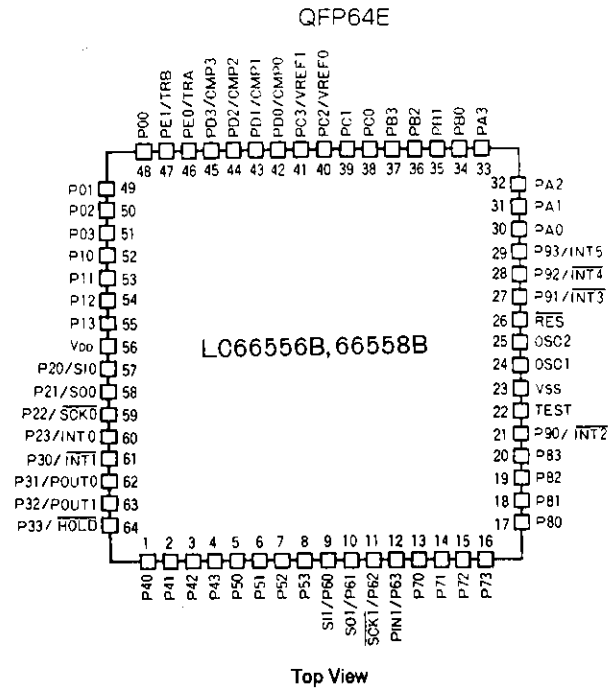
unit: mm

3159-QFP64E



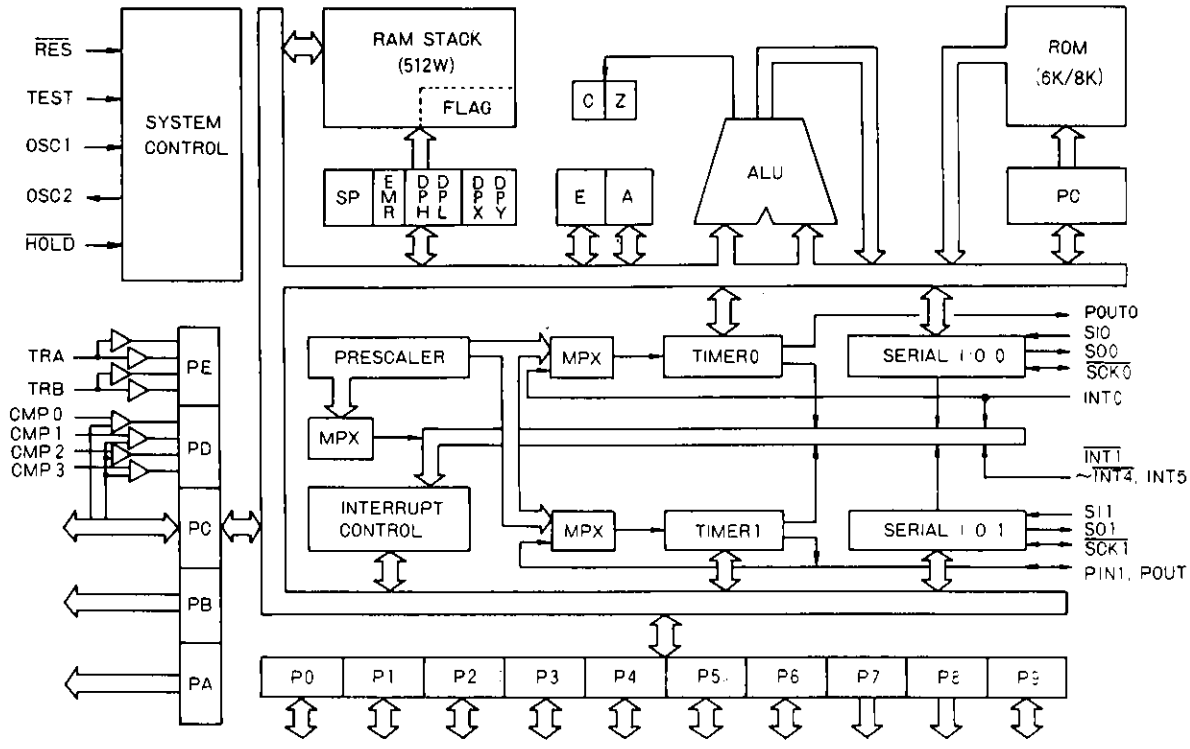
Pin Assignments





We recommend using reflow soldering as the QFP solder mounting technique.
Consult your Sanyo representative concerning temperature and other conditions if techniques in which the whole package is to be immersed in a solder dip bath, i.e. solder dip techniques, are to be used.

System Block Diagram



Differences between the LC66556B/LC66558B and the LC66508B Series

Item	LC66508B series (Including the EVA850/800-TB665XX tool)	LC66556B, 66558B
System differences • Hardware wait time (number of cycles) when hold mode is cleared	65536 cycles At 4 MHz (Tcyc = 1 µs): about 64 ms	16384 cycles At 4 MHz (Tcyc = 1 µs): about 16 ms
• Value of timer 0 at reset (including the value after hold mode is cleared)	The value FF0 is loaded.	The value FFC is loaded.
Differences in the major characteristics • Operating power supply voltage/operating speed	LC66512B, 516B 4.0 to 6.0 V/0.92 to 10 µs LC66E516, P516 4.5 to 5.5 V/0.92 to 10 µs	3.0 to 5.5V/0.92 to 10 µs

1. An RC oscillator cannot be used with the LC66556B and LC66558B
2. In addition, certain other output current and comparator input voltage specifications differ.
   For details, see the individual catalogs for the LC66508B, LC66E516 and LC66P516.
   Keep these differences in mind when using the LC66E516 and LC66P516 evaluation chips.

Pin Function Overview

Pin	I/O	Function	Output drive type	Option	Value on reset
P00 P01 P02 P03	I/O	I/O ports P00 to P03 • Input or output in 4-bit or 1-bit units • P00 to P03 have control functions in HALT mode.	• P-channel: pull-up MOS type • N-channel: small sink current type	• Either with pull-up MOS or N-channel OD output • Reset output level	High or low (option)
P10 P11 P12 P13	I/O	I/O ports P10 to P13 • Input or output in 4-bit or 1-bit units	• P-channel: pull-up MOS type • N-channel: small sink current type	• Either with pull-up MOS or N-channel OD output • Reset output level	High or low (option)
P20/SI0 P21/SO0 P22/$\overline{SCK0}$ P23/INT0	I/O	I/O ports P20 to P23 • Input or output in 4-bit or 1-bit units • P20 is also used as the serial input SI0 pin. P21 is also used as the serial output SO0 pin. P22 is also used as the serial clock $\overline{SCK0}$ pin. • P23 is also used as the INT0 interrupt request, as the timer 0 event counter and for pulse width measurement input.	• P-channel: CMOS type • N-channel: small sink current type • +15 V withstand voltage in N-channel OD	• Either CMOS or N-channel OD output	High
P30/$\overline{INT1}$ P31/POUT0 P32/POUT1	I/O	I/O ports P30 to P32 • Input or output in 3-bit or 1-bit units • P30 is also used as the $\overline{INT1}$ interrupt request. • P31 is also used for square wave output from timer 0. P32 is also used for square wave output from timer 1 and PWM output.	• P-channel: CMOS type • N-channel: small sink current type • +15 V withstand voltage in N-channel OD	• Either CMOS or N-channel OD output	High
P33/$\overline{HOLD}$	I	Hold mode control input • Hold mode is entered if a HOLD instruction is executed when $\overline{HOLD}$ is low. • When in hold mode, the CPU is reactivated by setting $\overline{HOLD}$ to the high level. • P33 can also be used as an input port together with P30 to P32. • When P33/$\overline{HOLD}$ is low, the CPU will not be reset by a low level on $\overline{RES}$. Therefore, $\overline{RES}$ cannot be used in applications that set P33/$\overline{HOLD}$ low when power is first applied.			
P40 P41 P42 P43	I/O	I/O ports P40 to P43 • Input or output in 4-bit or 1-bit units • I/O in 8-bit units when used in conjunction with P50 to P53 • Output of 8-bit ROM data when used in conjunction with P50 to P53	• P-channel: pull-up MOS type • N-channel: small sink current type	• Either CMOS or N-channel OD output	High
P50 P51 P52 P53	I/O	I/O ports P50 to P53 • Input or output in 4-bit or 1-bit units • I/O in 8-bit units when used in conjunction with P40 to P43 • Output of 8-bit ROM data when used in conjunction with P40 to P43	• P-channel: pull-up MOS type • N-channel: small sink current type	• Either CMOS or N-channel OD output	High

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Pin	I/O	Function	Output drive type	Option	Value on reset
P60/SI1 P61/SO1 P62/$\overline{SCK1}$ P63/PIN1	I/O	I/O ports P60 to P63 • Input or output in 4-bit or 1-bit units • P60 is also used as the serial input SI1 pin. • P61 is also used as the serial output SO1 pin. • P62 is also used as the serial clock $\overline{SCK1}$ pin. • P63 is also used as the timer 1 event counter input.	• P-channel: CMOS type • N-channel: small sink current type • +15 V withstand voltage in N-channel OD	• CMOS or N-channel OD output	High
P70 P71 P72 P73	O	Dedicated output ports P70 to P73 • Output in 4-bit or 1-bit units • The latched output data can be read with input instructions.	• P-channel: pull-up MOS type • N-channel: intermediate sink current type • +15 V withstand voltage in N-channel OD	• With pull-up MOS transistor or N-channel OD output	High
P80 P81 P82 P83	O	Dedicated output ports P80 to P83 • Output in 4-bit or 1-bit units • The latched output data can be read with input instructions. • A p-channel OD output option is available.	• P-channel: CMOS type • N-channel: small sink current type	• CMOS or P-channel OD output • The output level at reset	High or low (option)
P90/$\overline{INT2}$ P91/$\overline{INT3}$ P92/$\overline{INT4}$ P93/INT5	I/O	I/O ports P90 to P93 • Input or output in 4-bit or 1-bit units • P90 is also used as the $\overline{INT2}$ interrupt request. • P91 is also used as the $\overline{INT3}$ interrupt request. • P92 is also used as the $\overline{INT4}$ interrupt request. • P93 is also used as the INT5 interrupt request.	• P-channel: CMOS type • N-channel: small sink current type	• CMOS or N-channel OD output	High
PA0 PA1 PA2 PA3	O	Dedicated output ports PA0 to PA3 • Output in 4-bit or 1-bit units • The latched output data can be read with input instructions.	• P-channel: pull-up MOS type • N-channel: intermediate sink current type	• With pull-up MOS or N-channel OD output	High
PB0 PB1 PB2 PB3	O	Dedicated output ports PB0 to PB3 • Output in 4-bit or 1-bit units • The latched output data can be read with input instructions.	• P-channel: CMOS type • N-channel: small sink current type	• With pull-up MOS or N-channel OD output	High
PC0 PC1 PC2/VREF0 PC3/VREF1	I/O	I/O ports PC0 to PC3 • Input or output in 4-bit or 1-bit units • PC2 is also used as the VREF0 comparator comparison voltage pin. • PC3 is also used as the VREF1 comparator comparison voltage pin.		• CMOS or N-channel OD output	High
PD0/CMP0 PD1/CMP1 PD2/CMP2 PD3/CMP3	I	Dedicated input ports PD0 to PD3 • Can be switched to function as comparator inputs under software control. The comparison voltage for PD0 is VREF0. The comparison voltage for PD1 to PD3 is VREF1. Comparison can be specified in units of PD0, PD1, (PD2, PD3).			Normal input

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Pin	I/O	Function	Output drive type	Option	Value on reset
PE0/TRA PE1/TRB	I	Dedicated input port • Can be switched under software control to function as a three-value input port.			Normal input
OSC1 OSC2	I O	System clock oscillator connections When an external clock is used, leave OSC2 open and input the signal to OSC1.		• Selection of either a ceramic oscillator or external clock input	
$\overline{RES}$	I	System reset input • The CPU is initialized (reset) if a low level is input to $\overline{RES}$ when P33/$\overline{HOLD}$ is at the high level.			
TEST	I	CPU testing This pin must be connected to V_{SS} during normal operation.			
V_{DD} V_{SS}		Power supply connections			

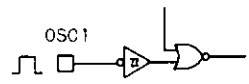
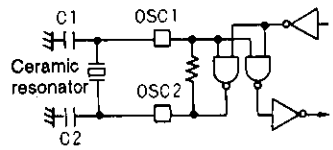
Note: Pull-up MOS output: An output with a pull-up MOS transistor
CMOS output: A complementary output
OD output: An open drain output

User Option Types

1. Port 0, 1 and 8 reset time output level option
   The output levels of I/O ports 0, 1 and 8 at reset can be selected from the following two options in 4-bit units.

Option	Conditions and notes
High level output at reset time	Ports 0, 1 and/or 8 in 4-bit sets
Low level output at reset time	Ports 0, 1 and/or 8 in 4-bit sets

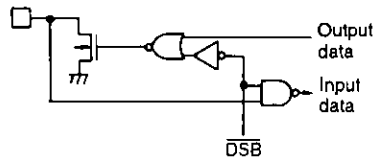
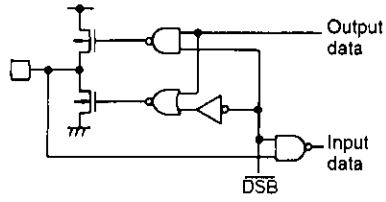
2. Oscillator circuit option

Option	Circuit	Conditions and notes
External clock		• This input is a Schmitt specification input.
Ceramic oscillator		

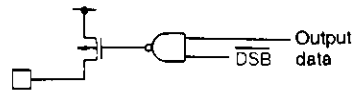
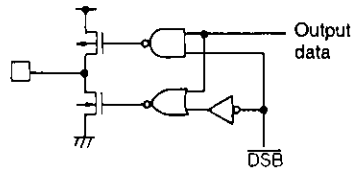
Note: There is no RC oscillator option.

3. Watchdog timer option
   The presence or absence of a program runaway detection function (watchdog timer) can be selected as an option.

4. Port output type option
   - One of the following two output circuit options can be selected for each bit in ports P0, P1, P2, P3 (except for the P33/$\overline{\text{HOLD}}$ pin), P4, P5, P6, P7, P9, PA, PB and PC.

Option	Circuit	Conditions and notes
Open drain output		P7, PA and PB are output only pins. P2, P3, P6 and P9 are Schmitt inputs.
Built-in pull-up resistor output		P7, PA and PB are output only pins. P2, P3, P6 and P9 are Schmitt inputs. CMOS outputs (P2, P3, P6, P9 and PC) and pull-up MOS outputs (P0, P1, P4, P5, P7, PA and PB) are differentiated.

   - The P8 circuits can be selected from the following two options in bit units.

Option	Circuit	Conditions and notes
Open drain output		
Built-in pull-up resistor output		

   - The PD comparator inputs and the PE three-value inputs are selected in software.

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit	Note
Maximum supply voltage	V_{DD} max	V_{DD}	−0.3 to +7.0	V	
Input voltage	V_{IN} (1)	P2, P3 (except for the P33/$\overline{HOLD}$ pin) and P6	−0.3 to +15.0	V	1
	V_{IN} (2)	Other inputs	−0.3 to V_{DD} + 0.3	V	2
Output voltage	V_{OUT} (1)	P2, P3 (except for the P33/$\overline{HOLD}$ pin), P6, P7 and PA	−0.3 to +15.0	V	1
	V_{OUT} (2)	Other outputs	−0.3 to V_{DD} + 0.3	V	2
Output current per pin	I_{ON} (1)	P0, P1, P2, P3 (except for the P33/$\overline{HOLD}$ pin), P4, P5, P6, P8, P9 and PC	4	mA	3
	I_{ON} (2)	P7, PA, PB	20	mA	3
	$-I_{OP}$ (1)	P0, P1, P4, P5, P7, PA, PB	2	mA	4
	$-I_{OP}$ (2)	P2, P3 (except for the P33/$\overline{HOLD}$ pin), P6, P8, P9 and PC	4	mA	4
Total pin current	ΣI_{ON} (1)	P2, P3 (except for the P33/$\overline{HOLD}$ pin), P4, P5, P6, P7 and P8	75	mA	3
	ΣI_{ON} (2)	P0, P1, P9, PA, PB, PC	75	mA	3
	$-\Sigma I_{OP}$ (1)	P2, P3 (except for the P33/$\overline{HOLD}$ pin), P4, P5, P6, P7 and P8	25	mA	4
	$-\Sigma I_{OP}$ (2)	P0, P1, P9, PA, PB, PC	25	mA	4
Allowable power dissipation	Pd max	Ta = −30 to +70°C: DIP64S (QIP64E)	600 (430)	mW	5
Operating temperature	Topr		−30 to +70	°C	
Storage temperature	Tstg		−55 to +125	°C	

Note: 1. Applies to open drain output specification pins. The rating from the "other pin" entry applies for specifications other than the open drain output specification.
2. Levels up to the free-running oscillation level are allowed for the oscillator input and output pins.
3. Inflow current (For P8, the CMOS output specifications apply.)
4. Outflow current (Applies to pull-up output specification and CMOS output specification pins except P8.)
5. We recommend using reflow soldering methods to mount the QFP package version.
Contact your Sanyo sales representative to discuss process conditions if techniques in which the whole package is immersed in a solder bath (solder dip or spray techniques) are used.

Allowable Operating Ranges at Ta = −30 to + 70°C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V unless specified otherwise

Parameter	Symbol	Conditions	min	typ	max	Unit	Note
Operating supply voltage	V_{DD}	V_{DD}	3.0		5.5	V	
Memory retention supply voltage	V_{DD} (H)	V_{DD}: In hold mode	1.8		5.5	V	
Input high level Voltage	V_{IH} (1)	P2, P3 (except for the P33/$\overline{HOLD}$ pin), P6: With the output n-channel transistor off	0.8 V_{DD}		13.5	V	1
	V_{IH} (2)	P33/$\overline{HOLD}$, P9, $\overline{RES}$, OSC1: With the output n-channel transistor off	0.8 V_{DD}		V_{DD}	V	2
	V_{IH} (3)	P0, P1, P4, P5, PC, PD, PE: With the output n-channel transistor off	0.75 V_{DD}		V_{DD}	V	3
	V_{IH} (4)	PE: When three-state input is used	0.8 V_{DD}		V_{DD}	V	
Intermediate level input voltage	V_{IM}	PE: When three-state input is used	0.4 V_{DD}		0.6 V_{DD}	V	
Common-mode input voltage range	V_{CMM} (1)	PD0, PC2: When comparator input is used	1.5		V_{DD}	V	
	V_{CMM} (2)	PD1, PD2, PD3, PC3: When comparator input is used	V_{SS}		V_{DD} − 1.5	V	
Low level input voltage	V_{IL} (1)	P2, P3 (except for the P33/$\overline{HOLD}$ pin), P6, P9, $\overline{RES}$, OSC1:N-channel output, transistor off	V_{SS}		0.2 V_{DD}	V	2
	V_{IL} (2)	P33/$\overline{HOLD}$: V_{DD} = 1.8 to 5.5 V	V_{SS}		0.2 V_{DD}	V	
	V_{IL} (3)	P0, P1, P4, P5, PC, PD, PE, TEST: N-channel output, transistor off	V_{SS}		0.25 V_{DD}	V	3
	V_{IL} (4)	PE: When three-state input is used	V_{SS}		0.2 V_{DD}	V	
Operating frequency (instruction cycle time)	fop (T_{CYC})		0.4 (10)		4.35 (0.92)	MHz (µs)	

Note: 1. Applies to open drain specification pins. However, the rating for V_{IH} (2) applies to the P33/$\overline{HOLD}$ pin. Ports P2, P3 and P6 cannot be used as input pins when CMOS output specifications are used.
2. Applies to open drain specification pins. P9, which has CMOS output specifications, can be used as input pins.
3. When PE is used as a three-value input, V_{IH} (4), V_{IM} and V_{IL} (4) apply. Port PC cannot be used as input pins when CMOS output specifications are used.

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Parameter	Symbol	Conditions	min	typ	max	Unit	Note
[External clock input conditions]							
Frequency	f_{ext}	OSC1: See Figure 1. With the signal input to OSC1 and with OSC2 open (with external clock input selected for the oscillator circuit option)	0.4		4.35	MHz	
Pulse width	t_{extH}, t_{extL}	OSC1: See Figure 1. With the signal input to OSC1 and with OSC2 open (with external clock input selected for the oscillator circuit option)	100			ns	
Rise and fall times	t_{extR}, t_{extF}	OSC1: See Figure 1. With the signal input to OSC1 and with OSC2 open (with external clock input selected for the oscillator circuit option)			30	ns	

Electrical Characteristics at Ta = –30 to + 70°C, V_{SS} = 0 V, V_{DD} = 3.0 to 5.5 V unless otherwise specified

Parameter	Symbol	Conditions	min	typ	max	Unit	Note
Input high level current	I_{IH} (1)	P2, P3 (except for the P33/$\overline{HOLD}$ pin), P6: V_{IN} = 13.5 V, N-channel output, transistor off			5.0	µA	1
	I_{IH} (2)	P0, P1, P4, P5, P9, PC, OSC1, $\overline{RES}$, P33/$\overline{HOLD}$ (except for PD, PE, PC2 and PC3): V_{IN} = V_{DD}, N-channel output, transistor off			1.0	µA	1
	I_{IH} (3)	PD, PE, PC2, PC3: V_{IN} = V_{DD}, N-channel output, transistor off			1.0	µA	1
Input low level current	I_{IL} (1)	Inputs other than PD, PE, PC2, PC3: V_{IN} = V_{SS}, N-channel output, transistor off	–1.0			µA	2
	I_{IL} (2)	PC2, PC3, PD, PE: V_{IN} = V_{SS}, N-channel output, transistor off	–1.0			µA	2
Output high level voltage	V_{OH} (1)	P2, P3 (except for the P33/$\overline{HOLD}$ pin), P6, P8, P9, PC: I_{OH} = –1 mA	V_{DD} – 1.0			V	3
		P2, P3 (except for the P33/$\overline{HOLD}$ pin), P6, P8, P9, PC: I_{OH} = –0.1 mA	V_{DD} – 0.5				
	V_{OH} (2)	P0, P1, P4, P5, P7, PA, PB: I_{OH} = –50 µA	V_{DD} – 1.0			V	4
		P0, P1, P4, P5, P7, PA, PB: I_{OH} = –30 µA	V_{DD} – 0.5				
Output pull-up current	I_{PO}	P0, P1, P4, P5, P7, PA, PB: V_{IN} = V_{SS}, V_{DD} = 5.5 V	–1.6			mA	4
Output low level voltage	V_{OL} (1)	P0, P1, P2, P3, P4, P5, P6, P8, P9, PC (except for the P33/$\overline{HOLD}$ pin): I_{OL} = 1.6 mA			0.4	V	5
	V_{OL} (2)	P7, PA, PB: I_{OL} = 8 mA			1.5	V	
Output off leakage current	I_{OFF} (1)	P2, P3, P6, P7, PA: V_{IN} = 13.5 V			5.0	µA	6
	I_{OFF} (2)	(except for P2, P3, P6, P7, P8 and PA): V_{IN} = V_{DD}			1.0	µA	6
	I_{OFF} (3)	P8: V_{IN} = V_{SS}	–1.0			µA	7
Comparator offset voltage	V_{OFF} (1)	PD1, PD2, PD3: V_{IN} = V_{SS} to V_{DD} – 1.5 V		±50	±300	mV	
	V_{OFF} (2)	PD0: V_{IN} = 1.5 V to V_{DD}		±50	±300	mV	
[Schmitt characteristics]							
Hysteresis voltage	V_{HIS}	P2, P3, $\overline{RES}$, P6, P9, OSC1, (RC, EXT)		0.1 V_{DD}		V	
High level threshold voltage	Vt H		0.5 V_{DD}		0.8 V_{DD}	V	
Low level threshold voltage	Vt L		0.2 V_{DD}		0.5 V_{DD}	V	
[Ceramic oscillator]							
Oscillator frequency	f_{CF}	OSC1, OSC2: See Figure 2, 4 MHz		4.0		MHz	
Oscillator stabilization time	t_{CFS}	See Figure 3, 4 MHz			10	ms	

Note: 1. Common input and output ports with open-drain output specifications are specified for the state with the output N-channel transistor turned off. These pins cannot be used for input when the CMOS output specification option is selected.
2. Common input and output ports with open-drain output specifications are specified for the state with the output N-channel transistor turned off. Ratings for pull-up output specification pins are stipulated for the output pull-up current IPO. These pins cannot be used for input when the CMOS output specification option is selected.
3. Stipulated for CMOS output specifications with the output N-channel transistor in the off state. (This also applies to P8 when P-channel open drain is selected.)
4. Stipulated for pull-up output specifications with the output N-channel transistor in the off state.
5. Stipulated for P8 with CMOS output specifications.
6. Stipulated for open drain output specifications with the output N-channel transistor in the off state.
7. Stipulated for open drain output specifications with the output P-channel transistor in the off state.

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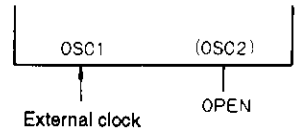
Parameter		Symbol	Conditions	min	typ	max	Unit	Note
[Serial clock]								
Cycle time	Input	t_{CKCY}	$\overline{SCK0}$, $\overline{SCK1}$: With the timing from Figure 4 and the test load from Figure 5	0.9			µs	
	Output			2.0			T_{CYC}	
Low level/high level pulse widths	Input	t_{CKL}		0.4			µs	
	Output	t_{CKH}		1.0			T_{CYC}	
Rise/fall times	Output	t_{CKR}, t_{CKF}				0.1	µs	
[Serial input]								
Data setup time		t_{ICK}	S10, SI1, SI0, SI1: With the timing in Figure 4. Stipulated with respect to the rising edge for $\overline{SCK0}$ and $\overline{SCK1}$.	0.3			µs	
Data hold time		t_{CKI}		0.3			µs	
[Serial output]								
Output delay time		t_{CKO}	SO0, SO1: With the timing from Figure 5 and the test load from Figure 5. Stipulated with respect to the falling edge for $\overline{SCK0}$ and $\overline{SCK1}$.			0.3	µs	
[Pulse input conditions]								
INT0 High and low level pulse widths		t_{I0H}, t_{I0L}	INT0, See Figure 6: Conditions such that the INT0 interrupt is accepted Conditions such that timer 0 event counter and pulse width measurement inputs are accepted	2			T_{CYC}	
High and low level pulse widths for interrupt inputs other than INT0		t_{I1H}, t_{I1L}	$\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, INT5, See Figure 6: Conditions such that all interrupts are accepted	2			T_{CYC}	
PIN1 High and low level pulse widths		t_{PINH}, t_{PINL}	PIN1, See Figure 6: Conditions such that timer 1 event counter inputs are accepted	2			T_{CYC}	
$\overline{RES}$ High and low level pulse widths		t_{RSH}, t_{RSL}	$\overline{RES}$, See Figure 6: Conditions such that reset can occur	3			T_{CYC}	
Comparator response speed		T_{RS}	PD, See Figure 7			20	ms	
Operating mode current drain		I_{DD} op	V_{DD}: 4 MHz ceramic oscillator		3.0	5.0	mA	8
			V_{DD}: 4 MHz external clock		3.0	5.0	mA	
HALT mode current drain		I_{DDHALT}	V_{DD}: 4 MHz ceramic oscillator		1.0	2.0	mA	
			V_{DD}: 4 MHz external clock		1.0	2.0	mA	
Hold mode current drain		I_{DDHOLD}	V_{DD}: V_{DD} = 1.8 to 5.5 V		0.01	10	µA	

Note: 8. Reset state



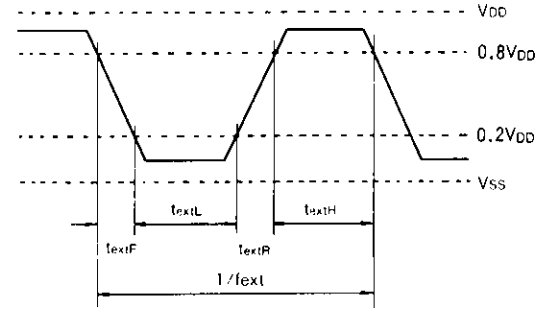


Figure 1 External Clock Input Waveform

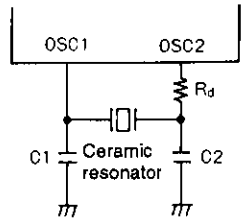


Figure 2 Ceramic Oscillator Circuit

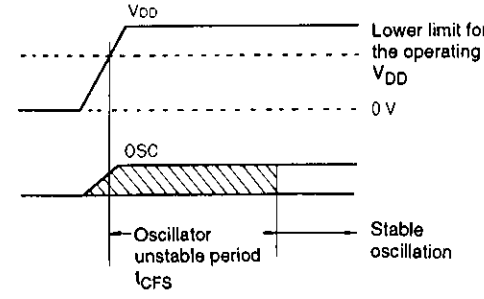


Figure 3 Oscillator Stabilization Period

Table 1 Ceramic Oscillator Guaranteed Constants

External capacitance	4 MHz (Murata Mfg. Co., Ltd.) CSA4.00MG	C1 = 33 pF ± 10%	4 MHz (Kyocera Corporation) KBR4.0 MS	C1 = 33 pF ± 10%
		C1 = 33 pF ± 10%		C1 = 33 pF ± 10%
		Rd = 0 Ω		Rd = 0 Ω
Internal capacitance	4 MHz (Murata Mfg. Co., Ltd.) CST4.00MG		4 MHz (Kyocera Corporation) KBR4.0MES	

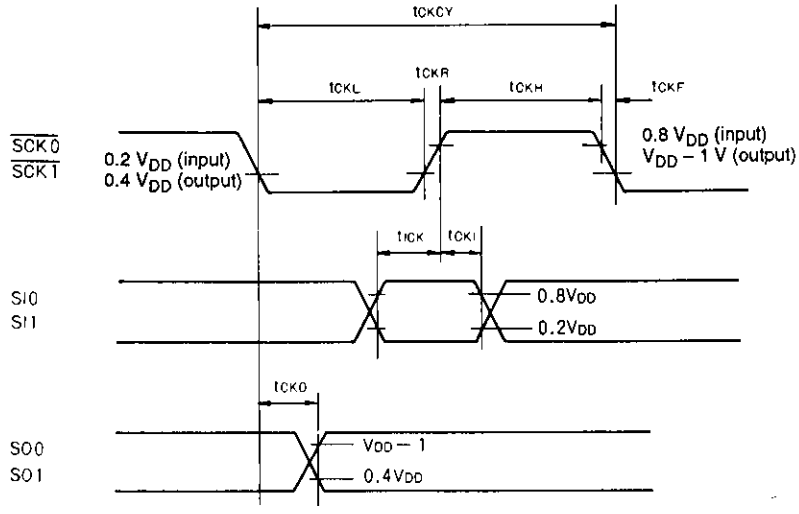


Figure 4 Serial I/O Timing

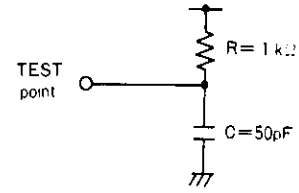


Figure 5 Timing Load

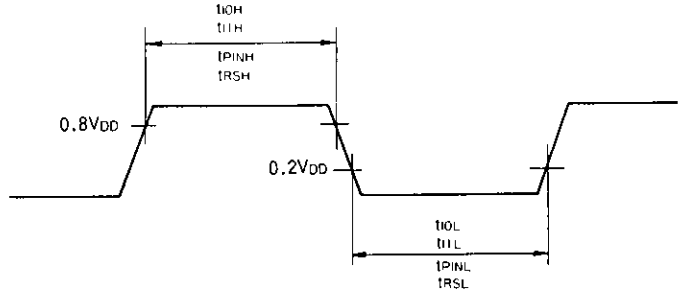


Figure 6 Input Timing for INT0, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, INT5, PIN1 and $\overline{RES}$

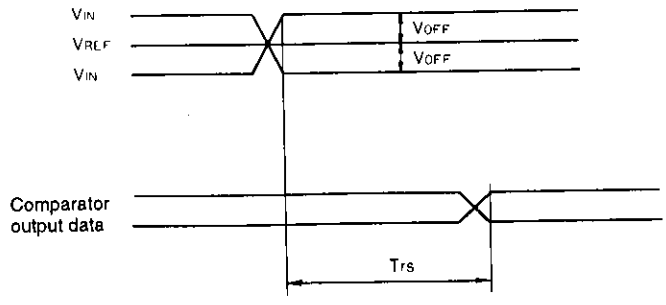
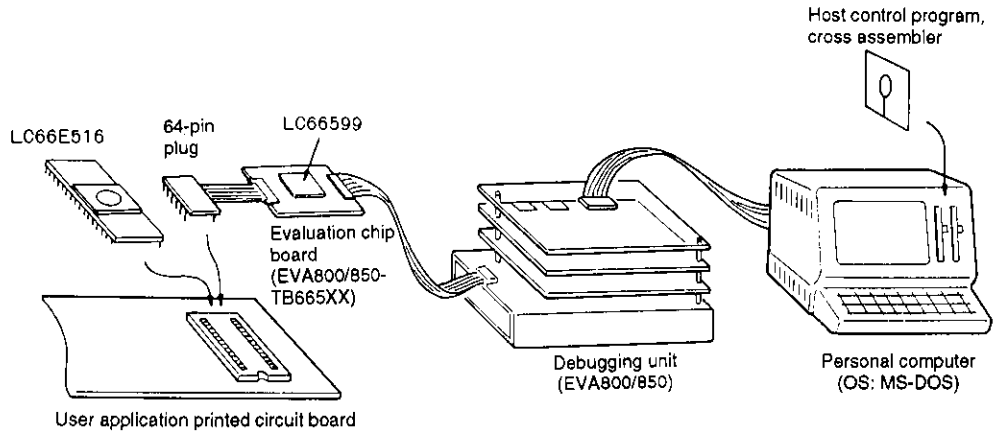


Figure 7 Comparator Response Speed Trs Timing

Application Development Tools

Programs for the LC66556B and LC66558B microprocessors are developed on an IBM-PC compatible personal computer running the MS-DOS operating system. A cross assembler and other tools are available. To make application development more convenient, Sanyo also provides a program debugging unit (EVA850/800), an evaluation board (EVA850/800-TB665XX), an evaluation chip (LC66599) and an on-chip EPROM microprocessor (LC66E516).



Structure of the Application Development Tools

1. Program debugging unit (EVA850/800)
   This is an emulator that provides functions for EPROM writing and serial data communications with external equipment (such as a host computer). It supports application development in machine language and program modification. Its main debugging functions include breaking, stepping and tracing. (The MPM665XX is used for the EVA850/800 monitor ROM.)
2. Evaluation chip board (EVA800/850-TB665XX)
   The evaluation chip signals and ports are output to the 64-pin connector and when the output cable is connected, the evaluation chip board converts these signals to the same pin assignments as those on the mass production chip. The evaluation chip board includes jumpers for setting options and other states and these jumper settings allow the evaluation chip to implement the same I/O circuit types and functions as the mass production chip. However, there are differences in the hold mode clear timing and the electrical characteristics.

Jumpers

Type	OSC		Reset method		Power supply to the user application board	
Jumper	Jumper 1 (J1)		Jumper 2 (J2:RES)		Jumper 3 (J3:V_{DD})	
Jumper setting and mode	EXT	External oscillator (external clock)	INT (a)	Reset by a RUN instruction from the host computer.	ON (a)	V_{DD} is supplied to the user application printed circuit board through the evaluation chip board.
	RC	RC oscillator	EXT (b)	Reset by the reset circuit on the user application printed circuit board.	OFF (b)	Separate power supplies on the user application printed circuit board and the evaluation chip board
	CF	CF oscillator				

Switches (SW1)

Type	Port 0, 1 and 8 output levels on reset						Watchdog timer presence or absence setting	
Switch	P0S		P1S		P8S		WDC	
Switch setting and mode	ON	Port 0 high	ON	Port 1 high	ON	Port 8 high	ON	Watchdog timer present
	OFF	Port 0 low	OFF	Port 1 low	OFF	Port 8 low	OFF	Watchdog timer absent

Note: Switches RC0 and RC1 must both be set to the on position.

Switches SW2 to SW14: Pull-up resistor option settings

1. Set the corresponding switch to the on position for built-in pull-up resistors and set the switch to the off position for open drain output. (SW10 is used for the port 8 pull-down resistor setting.)
2. These settings can be specified for individual pins.

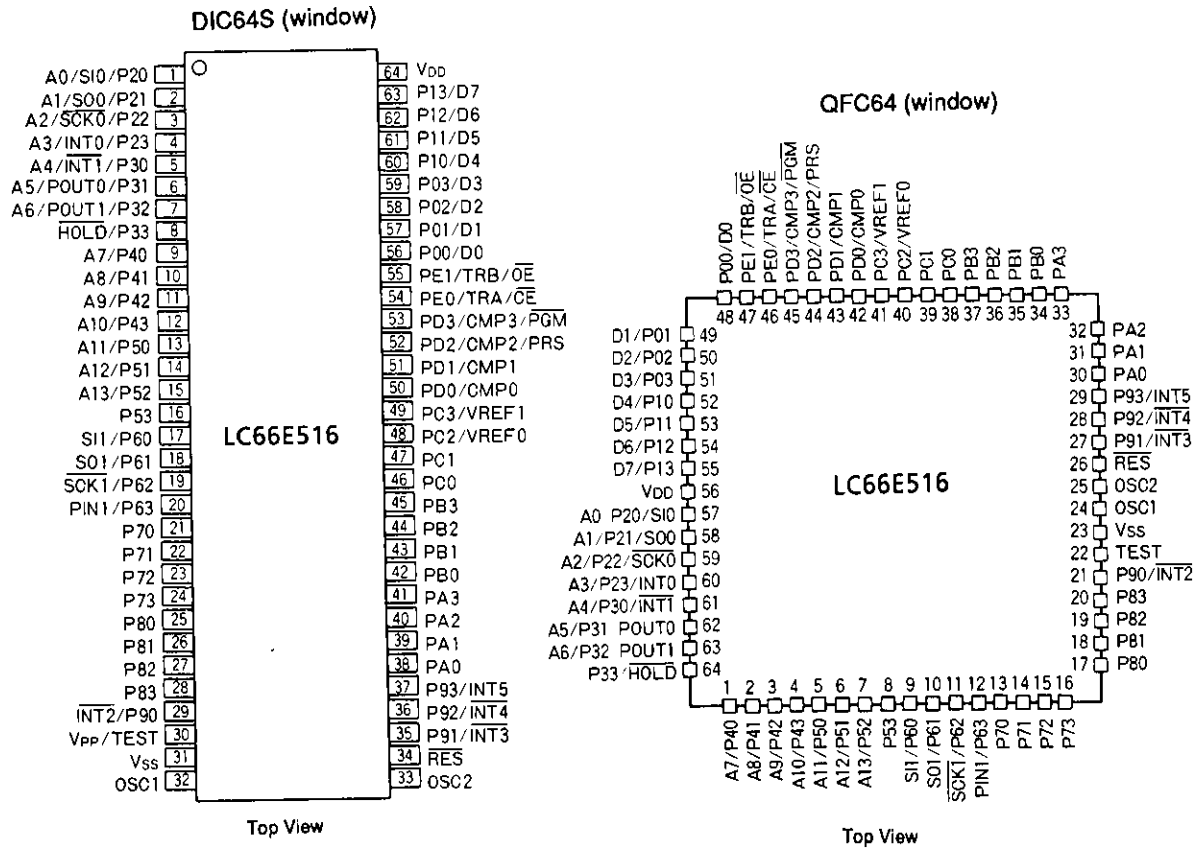
3. Cross assembler

Cross assembler (file name)	Object microprocessors	Limitations on program creation
LC66S. EXE	LC66562B/566B (LC66E516/P516) (LC66599)	SB instruction limitations • LC66556B: SB0, SB1, SB2 and SB3 cannot be used • LC66558B: SB0, SB1, SB2 and SB3 cannot be used • LC66E516/P516: SB0, SB1, SB2 and SB3 can be used • LC66599: SB0, SB1, SB2 and SB3 can be used

4. Simulation chip (See the LC66E516 individual product catalog for more details.)
   The LC66E516 simulation chip is an on-chip EPROM microprocessor. Mounted configuration operation can be confirmed in the application product by using a dedicated conversion board (the W66E516DH for DIC products and the W66E516QH for QFP products) and writing programs with a commercial PROM writer.

   • Form
   The LC66E516 has a pin assignment and functions identical to those of the LC66556B and LC66558B. However, there are differences in the hold mode clear timing and the electrical characteristics. The figure below shows the pin assignment .
   The figure below shows the pin assignment .
   • Options
   The options (the port 0, 1 and 8 levels at reset, the watchdog timer and the port output circuit types) for the microprocessor to be evaluated can be specified by EPROM data. This allows evaluation with the same peripheral circuits as those that will be used in the mass production product.

Pin Assignments



LC665XX Series Instruction Table (by function)

Abbreviations:

AC: Accumulator
E: E register
CF: Carry flag
ZF: Zero flag
HL: Data pointer DPH, DPL
XY: Data pointer DPX, DPY
M: Data memory
M (HL): Data memory pointed to by the DPH, DPL data pointer
M (XY): Data memory pointed to by the DPX, DPY auxiliary data pointer
M2 (HL): Two words of data memory (starting on an even address) pointed to by the DPH, DPL data pointer
SP: Stack pointer
M2 (SP): Two words of data memory pointed to by the stack pointer
M4 (SP): Four words of data memory pointed to by the stack pointer
in: n bits of immediate data
t2: Bit specification

t2	11	10	01	00
Bit	2^3	2^2	2^1	2^0

PCh: Bits 8 to 11 in the PC
PCm: Bits 4 to 7 in the PC
PCl: Bits 0 to 3 in the PC
Fn: User flag, n = 0 to 15
TIMER0: Timer 0
TIMER1: Timer 1
SIO: Serial register
P: Port
P (i4): Port indicated by 4 bits of immediate data
INT: Interrupt enable flag
( ), [ ]: Indicates the contents of a location
←: Transfer direction, result
∨: Exclusive or
∧: Logical and
∨: Logical or
+: Addition
−: Subtraction
—: Taking the one's complement

Mnemonic		Instruction code		Number of bytes	Number of cycles	Operation	Description	Affected status bits	Note
		D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0						
[Accumulator manipulation instructions]									
CLA	Clear AC	1 0 0 0	0 0 0 0	1	1	AC ← 0 (Equivalent to LAI 0.)	Clear AC.	ZF	Has a vertical skip function.
DAA	Decimal adjust AC in addition	1 1 0 0 0 0 1 0	1 1 1 1 0 1 1 0	2	2	AC ← (AC) + 6 (Equivalent to ADI 6.)	Add six to AC.	ZF	
DAS	Decimal adjust AC in subtraction	1 1 0 0 0 0 1 0	1 1 1 1 1 0 1 0	2	2	AC ← (AC) + 10 (Equivalent to ADI 0AH.)	Add 10 to AC.	ZF	
CLC	Clear CF	0 0 0 1	1 1 1 0	1	1	CF ← 0	Clear CF to 0.	CF	
STC	Set CF	0 0 0 1	1 1 1 1	1	1	CF ← 1	Set CF to 1.	CF	
CMA	Complement AC	0 0 0 1	1 0 0 0	1	1	AC ← $\overline{(AC)}$	Take the one's complement of AC.	ZF	
IA	Increment AC	0 0 0 1	0 1 0 0	1	1	AC ← (AC) + 1	Increment AC.	ZF, CF	
DA	Decrement AC	0 0 1 0	0 1 0 0	1	1	AC ← (AC) − 1	Decrement AC.	ZF, CF	
RAR	Rotate AC right through CF	0 0 0 1	0 0 0 0	1	1	AC_3 ← (CF), ACn ← (ACn + 1), CF ← (AC_0)	Shift AC (including CF) right.	CF	
RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC_0 ← (CF), ACn + 1 ← (ACn), CF ← (AC_3)	Shift AC (including CF) left.	CF, ZF	
TAE	Transfer AC to E	0 1 0 0	0 1 0 1	1	1	E ← (AC)	Move the contents of AC to E.		
TEA	Transfer E to AC	0 1 0 0	0 1 1 0	1	1	AC ← (E)	Move the contents of E to AC.	ZF	
XAE	Exchange AC with E	0 1 0 0	0 1 0 0	1	1	(AC) ↔ (E)	Exchange the contents of AC and E.		
[Memory manipulation instructions]									
IM	Increment M	0 0 0 1	0 0 1 0	1	1	M (HL) ← [M (HL)] + 1	Increment M (HL).	ZF, CF	
DM	Decrement M	0 0 1 0	0 0 1 0	1	1	M (HL) ← [M (HL)] − 1	Decrement M (HL).	ZF, CF	
IMDR i8	Increment M direct	1 1 0 0 I_7 I_6 I_5 I_4	0 1 1 1 I_3 I_2 I_1 I_0	2	2	M (i8) ← [M (i8)] + 1	Increment M (i8).	ZF, CF	
DMDR i8	Decrement M direct	1 1 0 0 I_7 I_6 I_5 I_4	0 0 1 1 I_3 I_2 I_1 I_0	2	2	M (i8) ← [M (i8)] − 1	Decrement M (i8).	ZF, CF	
SMB t2	Set M data bit	0 0 0 0	1 1 t_1 t_0	1	1	[M (HL), t2] ← 1	Set the bit in M (HL) specified by t0 and t1 to 1.		
RMB t2	Reset M data bit	0 0 1 0	1 1 t_1 t_0	1	1	[M (HL), t2] ← 0	Clear the bit in M (HL) specified by t0 and t1 to 0.	ZF	
[Arithmetic, logic and comparison instructions]									
AD	Add M to AC	0 0 0 0	0 1 1 0	1	1	AC ← (AC) + [M (HL)]	Add the contents of AC and M (HL) as two's complement values and store the result in AC.	ZF, CF	
ADDR i8	Add M direct to AC	1 1 0 0 I_7 I_6 I_5 I_4	1 0 0 1 I_3 I_2 I_1 I_0	2	2	AC ← (AC) + [M (i8)]	Add the contents of AC and M (i8) as two's complement values and store the result in AC.	ZF, CF	
ADC	Add M to AC with CF	0 0 0 0	0 0 1 0	1	1	AC ← (AC) + [M (HL)] + (CF)	Add the contents of AC, M (HL) and CF as two's complement values and store the result in AC.	ZF, CF	
ADI i4	Add immediate data to AC	1 1 0 0 0 0 1 0	1 1 1 1 I_3 I_2 I_1 I_0	2	2	AC ← (AC) + I_3, I_2, I_1, I_0	Add the contents of AC and the immediate data as two's complement values and store the result in AC.	ZF	
SUBC	Subtract AC from M with CF	0 0 0 1	0 1 1 1	1	1	AC ← [M (HL)] − (AC) − (CF)	Subtract the contents of AC and $\overline{CF}$ from M (HL) as two's complement values and store the result in AC.	ZF, CF	CF will be zero if there was a borrow and one otherwise.
ANDA	And M with AC then store AC	0 0 0 0	0 1 1 1	1	1	AC ← (AC) ∧ [M (HL)]	Take the logical and of AC and M (HL) and store the result in AC.	ZF	
ORA	Or M with AC then store AC	0 0 0 0	0 1 0 1	1	1	AC ← (AC) ∨ [M (HL)]	Take the logical or of AC and M (HL) and store the result in AC.	ZF	

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Mnemonic		Instruction code		Number of bytes	Number of cycles	Operation	Description	Affected status bits	Note
		D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0						
[Arithmetic, logic and comparison instructions]									
EXL	Exclusive or M with AC then store AC	0 0 0 1	0 1 0 1	1	1	AC ← (AC) ∀ [M (HL)]	Take the logical exclusive or of AC and M (HL) and store the result in AC.	ZF	
ANDM	And M with AC then store M	0 0 0 0	0 0 1 1	1	1	M (HL) ← (AC) ∧ [M (HL)]	Take the logical and of AC and M (HL) and store the result in M (HL).	ZF	
ORM	Or M with AC then store M	0 0 0 0	0 1 0 0	1	1	M (HL) ← (AC) ∨ [M (HL)]	Take the logical or of AC and M (HL) and store the result in M (HL).	ZF	
CM	Compare AC with M	0 0 0 1	0 1 1 0	1	1	$\overline{[M\ (HL)]}$ + (AC) + 1	Compare the contents of AC and M (HL) and set or clear CF and ZF according to the result. Magnitude comparison / CF / ZF [M (HL)] > (AC) 0 0 [M (HL)] = (AC) 1 1 [M (HL)] < (AC) 1 0	ZF, CF	
CI i4	Compare AC with immediate data	1 1 0 0 1 0 1 0	1 1 1 1 I_3 I_2 I_1 I_0	2	2	$\overline{I_3\ I_2\ I_1\ I_0}$ + (AC) + 1	Compare the contents of AC and the immediate data I_3 I_2 I_1 I_0 and set or clear CF and ZF according to the result. Magnitude comparison / CF / ZF I_3 I_2 I_1 I_0 > AC 0 0 I_3 I_2 I_1 I_0 = AC 1 1 I_3 I_2 I_1 I_0 < AC 1 0	ZF, CF	
CLI i4	Compare DP_L with immediate data	1 1 0 0 1 0 1 1	1 1 1 1 I_3 I_2 I_1 I_0	2	2	ZF ← 1 if (DP_L) = I_3 I_2 I_1 I_0 ZF ← 0 if (DP_L) ≠ I_3 I_2 I_1 I_0	Compare the contents of DP_L with the immediate data. Set ZF if identical and clear ZF if not.	ZF	
CMB t2	Compare AC bit with M data bit	1 1 0 0 1 1 0 1	1 1 1 1 0 0 t_1 t_0	2	2	ZF ← 1 if (AC, t2) = [M (HL), t2] ZF ← 0 if (AC, t2) ≠ [M (HL), t2]	Compare the corresponding bits specified by t0 and t1 in AC and M (HL). Set ZF if identical and clear ZF if not.	ZF	
[Load and store instructions]									
LAE	Load AC and E from M2 (HL)	0 1 0 1	1 1 0 0	1	1	AC ← M (HL), E ← M (HL + 1)	Load the contents of M2 (HL) into AC, E.		
LAI i4	Load AC with Immediate data	1 0 0 0	I_3 I_2 I_1 I_0	1	1	AC ← I_3 I_2 I_1 I_0	Load the immediate data into AC.	ZF	Has a vertical skip function
LADR i8	Load AC from M direct	1 1 0 0 I_7 I_6 I_5 I_4	0 0 0 1 I_3 I_2 I_1 I_0	2	2	AC ← [M (i8)]	Load the contents of M (i8) into AC.	ZF	
S	Store AC to M	0 1 0 0	0 1 1 1	1	1	M (HL) ← (AC)	Store the contents of AC into M (HL).		
SAE	Store AC and E to M2 (HL)	0 1 0 1	1 1 1 0	1	1	M (HL) ← (AC) M (HL + 1) ← (E)	Store the contents of AC, E into M2 (HL).		
LA reg	Load AC from M (reg)	0 1 0 0	1 0 t_0 0	1	1	AC ← [M (reg)]	Load the contents of M (reg) into AC. The reg is either HL or XY depending on t_0. reg / t_0 HL 0 XY 1	ZF	

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Mnemonic		Instruction code $D_7\ D_6\ D_5\ D_4$	Instruction code $D_3\ D_2\ D_1\ D_0$	Number of bytes	Number of cycles	Operation	Description	Affected status bits	Note
[Load and store instructions]									
LA reg, I	Load AC from M (reg) then increment reg	0 1 0 0	1 0 t_0 1	1	2	AC ← [M (reg)] DP_L ← (DP_L) + 1 or DP_Y ← (DP_Y) + 1	Load the contents of M (reg) into AC. (The reg is either HL or XY.) Then increment the contents of either DP_L or DP_Y. The relationship between t_0 and reg is the same as that for the LA reg instruction.	ZF	ZF is set according to the result of incrementing DP_L or DP_Y.
LA reg, D	Load AC from M (reg) then decrement reg	0 1 0 1	1 0 t_0 1	1	2	AC ← [M (reg)] DP_L ← (DP_L) − 1 or DP_Y ← (DP_Y) − 1	Load the contents of M (reg) into AC. (The reg is either HL or XY.) Then decrement the contents of either DP_L or DP_Y. The relationship between t_0 and reg is the same as that for the LA reg instruction.	ZF	ZF is set according to the result of decrementing DP_L or DP_Y.
XA reg	Exchange AC with M (reg)	0 1 0 0	1 1 t_0 0	1	1	(AC) ← [M (reg)]	Exchange the contents of M (reg) and AC. The reg is either HL or XY depending on t_0. reg: HL → t_0 = 0; XY → t_0 = 1		
XA reg, I	Exchange AC with M (reg) then increment reg	0 1 0 0	1 1 t_0 1	1	2	(AC) ← [M (reg)] DP_L ← (DP_L) + 1 or DP_Y ← (DP_Y) + 1	Exchange the contents of M (reg) and AC. (The reg is either HL or XY.) Then increment the contents of either DP_L or DP_Y. The relationship between t_0 and reg is the as that for the XA reg instruction.	ZF	ZF is set according to the result of incrementing DP_L or DP_Y.
XA reg, D	Exchange AC with M (reg) then decrement reg	0 1 0 1	1 1 t_0 1	1	2	(AC) ← [M (reg)] DP_L ← (DP_L) − 1 or DP_Y ← (DP_Y) − 1	Exchange the contents of M (reg) and AC. (The reg is either HL or XY.) Then decrement the contents of either DP_L or DP_Y. The relationship between t_0 and reg is the as that for the XA reg instruction.	ZF	ZF is set according to the result of decrementing DP_L or DP_Y.
XADR i8	Exchange AC with M direct	1 1 0 0 $I_7\ I_6\ I_5\ I_4$	1 0 0 0 $I_3\ I_2\ I_1\ I_0$	2	2	(AC) ← [M (i8)]	Exchange the contents of AC and M (i8).		
LEAI i8	Load E & AC with immediate data	1 1 0 0 $I_7\ I_6\ I_5\ I_4$	0 1 1 0 $I_3\ I_2\ I_1\ I_0$	2	2	E ← $I_7\ I_6\ I_5\ I_4$ AC ← $I_3\ I_2\ I_1\ I_0$	Load the immediate data i8 into E, AC.		
RTBL	Read table data from program ROM	0 1 0 1	1 0 1 0	1	2	E, AC ← [ROM (PCh, E, AC)]	Load into E, AC the ROM data at the location determined by replacing the lower 8 bits of the PC with E, AC.		
RTBLP	Read table data from program ROM then output to P4, 5	0 1 0 1	1 0 0 0	1	2	Port 4, 5 ← [ROM (PCh, E, AC)]	Output from ports 4 and 5 the ROM data at the location determined by replacing the lower 8 bits of the PC with E, AC.		
[Data pointer manipulation instructions]									
LDZ i4	Load DP_H with zero and DP_L with immediate data respectively	0 1 1 0	$I_3\ I_2\ I_1\ I_0$	1	1	DP_H ← 0 DPL ← $I_3\ I_2\ I_1\ I_0$	Load zero into DP_H and the immediate data i4 into DP_L.		
LHI i4	Load DP_H with immediate data	1 1 0 0 0 0 0 0	1 1 1 1 $I_3\ I_2\ I_1\ I_0$	2	2	DP_H ← $I_3\ I_2\ I_1\ I_0$	Load the immediate data i4 into DP_H.		
LLI i4	Load DP_L with immediate data	1 1 0 0 0 0 0 1	1 1 1 1 $I_3\ I_2\ I_1\ I_0$	2	2	DP_L ← $I_3\ I_2\ I_1\ I_0$	Load the immediate data i4 into DP_L.		
LHLI i8	Load DP_H, DP_L with immediate data	1 1 0 0 $I_7\ I_6\ I_5\ I_4$	0 0 0 0 $I_3\ I_2\ I_1\ I_0$	2	2	DP_H ← $I_7\ I_6\ I_5\ I_4$ DP_L ← $I_3\ I_2\ I_1\ I_0$	Load the Immediate data into DL_H, DP_L.		
LXYI i8	Load DP_X, DP_Y with immediate data	1 1 0 0 $I_7\ I_6\ I_5\ I_4$	0 0 1 0 $I_3\ I_2\ I_1\ I_0$	2	2	DP_X ← $I_7\ I_6\ I_5\ I_4$ DP_Y ← $I_3\ I_2\ I_1\ I_0$	Load the immediate data Into DL_X, DP_Y.		

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Mnemonic		Instruction code $D_7 D_6 D_5 D_4$	Instruction code $D_3 D_2 D_1 D_0$	Number of bytes	Number of cycles	Operation	Description	Affected status bits	Note
[Data pointer manipulation instructions]									
IL	Increment DP_L	0 0 0 1	0 0 0 1	1	1	$DP_L \leftarrow (DP_L) + 1$	Increment the contents of DP_L.	ZF	
DL	Decrement DP_L	0 0 1 0	0 0 0 1	1	1	$DP_L \leftarrow (DP_L) - 1$	Decrement the contents of DP_L.	ZF	
IY	Increment DP_Y	0 0 0 1	0 0 1 1	1	1	$DP_Y \leftarrow (DP_Y) + 1$	Increment the contents of DP_Y.	ZF	
DY	Decrement DP_Y	0 0 1 0	0 0 1 1	1	1	$DP_Y \leftarrow (DP_Y) - 1$	Decrement the contents of DP_Y.	ZF	
TAH	Transfer AC to DP_H	1 1 0 0 1 1 1 1	1 1 1 1 0 0 0 0	2	2	$DP_H \leftarrow (AC)$	Transfer the contents of AC to DP_H.		
THA	Transfer DP_H to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 0 0	2	2	$AC \leftarrow (DP_H)$	Transfer the contents of DP_H to AC.	ZF	
XAH	Exchange AC with DP_H	0 1 0 0	0 0 0 0	1	1	$(AC) \leftrightarrow (DP_H)$	Exchange the contents of AC and DP_H.		
TAL	Transfer AC to DP_L	1 1 0 0 1 1 1 1	1 1 1 1 0 0 0 1	2	2	$DP_L \leftarrow (AC)$	Transfer the contents of AC to DP_L.		
TLA	Transfer DP_L to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 0 1	2	2	$AC \leftarrow (DP_L)$	Transfer the contents of DP_L to AC.	ZF	
XAL	Exchange AC with DP_L	0 1 0 0	0 0 0 1	1	1	$(AC) \leftrightarrow (DP_L)$	Exchange the contents of AC and DP_L.		
TAX	Transfer AC to DP_X	1 1 0 0 1 1 1 1	1 1 1 1 0 0 1 0	2	2	$DP_X \leftarrow (AC)$	Transfer the contents of AC to DP_X.		
TXA	Transfer DP_X to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 1 0	2	2	$AC \leftarrow (DP_X)$	Transfer the contents of DP_X to AC.	ZF	
XAX	Exchange AC with DP_X	0 1 0 0	0 0 1 0	1	1	$(AC) \leftrightarrow (DP_X)$	Exchange the contents of AC and DP_X.		
TAY	Transfer AC to DP_Y	1 1 0 0 1 1 1 1	1 1 1 1 0 0 1 1	2	2	$DP_Y \leftarrow (AC)$	Transfer the contents of AC to DP_Y.		
TYA	Transfer DP_Y to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 1 1	2	2	$AC \leftarrow (DP_Y)$	Transfer the contents of DP_Y to AC.	ZF	
XAY	Exchange AC with DP_Y	0 1 0 0	0 0 1 1	1	1	$(AC) \leftrightarrow (DP_Y)$	Exchange the contents of AC and DP_Y.		
[Flag manipulation instructions]									
SFB n4	Set flag bit	0 1 1 1	$n_3 n_2 n_1 n_0$	1	1	$Fn \leftarrow 1$	Set the flag specified by n4 to 1.		
RFB n4	Reset flag bit	0 0 1 1	$n_3 n_2 n_1 n_0$	1	1	$Fn \leftarrow 0$	Reset the flag specified by n4 to 0.	ZF	
[Jump and subroutine instructions]									
JMP addr	Jump in the current bank	1 1 1 0 $P_7 P_6 P_5 P_4$	$P_{11} P_{10} P_9 P_8$ $P_3 P_2 P_1 P_0$	2	2	PC13, 12 ← PC13, 12 PC11 to 0 ← P_{11} to P_0	Jump to the location in the same bank specified by the immediate data P12.		This becomes PC12 + $\overline{(PC12)}$ immediately following a BANK Instruction.
JPEA	Jump to the address stored at E and AC in the current page	0 0 1 0	0 1 1 1	1	1	PC13 to 8 ← PC13 to 8, PC7 to 4 ← (E), PC3 to 0 ← (AC)	Jump to the location determined by replacing the lower 8 bits of the PC by E, AC.		
CAL addr	Call subroutine	0 1 0 1 $P_7 P_6 P_5 P_4$	0 $P_{10} P_9 P_8$ $P_3 P_2 P_1 P_0$	2	2	PC13 to 11 ← 0, PC10 to 0 ← P_{10} to P_0, M4 (SP) ← (CF, ZF, PC13 to 0), SP ← (SP)-4	Call a subroutine.		
CZP addr	Call subroutine in the zero page	1 0 1 0	$P_3 P_2 P_1 P_0$	1	2	PC13 to 6, PC10 ← 0, PC5 to 2 ← P_3 to P_0, M4 (SP) ← (CF, ZF, PC12 to 0), SP ← SP-4	Call a subroutine on page 0 in bank 0.		
BANK	Change bank	0 0 0 1	1 0 1 1	1	1		Change the memory bank and register bank.		

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Mnemonic		Instruction code		Number of bytes	Number of cycles	Operation	Description	Affected status bits	Note
		$D_7\ D_6\ D_5\ D_4$	$D_3\ D_2\ D_1\ D_0$						
[Jump and subroutine instructions]									
PUSH reg	Push reg on M2 (SP)	1 1 0 0 1 1 1 1	1 1 1 1 1 i_1 i_0 0	2	2	M2 (SP) ← (reg) SP ← (SP)-2	Store the contents of reg in M2 (SP). Subtract 2 from SP after the store. reg: HL (i_1 i_0 = 0 0), XY (0 1), AE (1 0), Illegal (1 1)		
POP reg	Pop reg off M2 (SP)	1 1 0 0 1 1 1 0	1 1 1 1 1 i_1 i_0 0	2	2	SP ← (SP) + 2 reg ← [M2 (SP)]	Add 2 to SP and then load the contents of M2(SP) into reg. The relation between i1i0 and reg is the same as that for the PUSH reg instruction.		
RT	Return from subroutine	0 0 0 1	1 1 0 0	1	2	SP ← (SP) + 4 PC ← [M4 (SP)]	Return from a subroutine or interrupt handling routine. ZF and CF are not restored.		
RTI	Return from interrupt routine	0 0 0 1	1 1 0 1	1	2	SP ← (SP) + 4 PC ← [M4 (SP)] CF, ZF ← [M4 (SP)]	Return from a subroutine or interrupt handling routine. ZF and CF are restored.	ZF, CF	
[Branch instructions]									
BAt2 addr	Branch on AC bit	1 1 0 1 $P_7\ P_6\ P_5\ P_4$	0 0 t_1 t_0 $P_3\ P_2\ P_1\ P_0$	2	2	PC7 to 0 ← $P_7\ P_6\ P_5\ P_4$ $P_3\ P_2\ P_1\ P_0$ if (AC, t2) = 1	Branch to the location in the same page specified by P_7 to P_0 if the bit in AC specified by the immediate data t_1 t_0 is 1.		
BNAt2 addr	Branch on no AC bit	1 0 0 1 $P_7\ P_6\ P_5\ P_4$	0 0 t_1 t_0 $P_3\ P_2\ P_1\ P_0$	2	2	PC7 to 0 ← $P_7\ P_6\ P_5\ P_4$ $P_3\ P_2\ P_1\ P_0$ if (AC, t2) = 0	Branch to the location in the same page specified by P_7 to P_0 if the bit in AC specified by the immediate data t_1 t_0 is 0.		
BMt2 addr	Branch on M bit	1 1 0 1 $P_7\ P_6\ P_5\ P_4$	0 1 t_1 t_0 $P_3\ P_2\ P_1\ P_0$	2	2	PC7 to 0 ← $P_7\ P_6\ P_5\ P_4$ $P_3\ P_2\ P_1\ P_0$ if [M (HL),t2] = 1	Branch to the location in the same page specified by P_7 to P_0 if the bit in M (HL) specified by the immediate data t_1 t_0 is 1.		
BNMt2 addr	Branch on no M bit	1 0 0 1 $P_7\ P_6\ P_5\ P_4$	0 1 t_1 t_0 $P_3\ P_2\ P_1\ P_0$	2	2	PC7 to 0 ← $P_7\ P_6\ P_5\ P_4$ $P_3\ P_2\ P_1\ P_0$ if [M (HL),t2] = 0	Branch to the location in the same page specified by P_7 to P_0 if the bit in M (HL) specified by the immediate data t_1 t_0 is 0.		
BPt2 addr	Branch on Port bit	1 1 0 1 $P_7\ P_6\ P_5\ P_4$	1 0 t_1 t_0 $P_3\ P_2\ P_1\ P_0$	2	2	PC7 to 0 ← $P_7\ P_6\ P_5\ P_4$ $P_3\ P_2\ P_1\ P_0$ if [P (DP_L), t2] = 1	Branch to the location in the same page specified by P_7 to P_0 if the bit in port (DP_L) specified by the immediate data t_1 t_0 is 1.		Internal control registers can also be tested by executing this instruction immediately after a BANK instruction. However, this is limited to registers that can be read out.
BNPt2 addr	Branch on no Port bit	1 0 0 1 $P_7\ P_6\ P_5\ P_4$	1 0 t_1 t_0 $P_3\ P_2\ P_1\ P_0$	2	2	PC7 to 0 ← $P_7\ P_6\ P_5\ P_4$ $P_3\ P_2\ P_1\ P_0$ if [P (DP_L), t2] = 0	Branch to the location in the same page specified by P_7 to P_0 if the bit in port (DP_L) specified by the immediate data t_1 t_0 is 0.		Internal control registers can also be tested by executing this instruction immediately after a BANK instruction. However, this is limited to registers that can be read out.

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Mnemonic		Instruction code		Number of bytes	Number of cycles	Operation	Description	Affected status bits	Note
		$D_7\ D_6\ D_5\ D_4$	$D_3\ D_2\ D_1\ D_0$						
[Branch instructions]									
BC addr	Branch on CF	1 1 0 1 $P_7\ P_6\ P_5\ P_4$	1 1 0 0 $P_3\ P_2\ P_1\ P_0$	2	2	PC7 to 0 ← $P_7\ P_6\ P_5\ P_4$ $P_3\ P_2\ P_1\ P_0$ if (CF) = 1	Branch to the location in the same page specified by P_7 to P_0 if CF is 1		
BNC addr	Branch on no CF	1 0 0 1 $P_7\ P_6\ P_5\ P_4$	1 1 0 0 $P_3\ P_2\ P_1\ P_0$	2	2	PC7 to 0 ← $P_7\ P_6\ P_5\ P_4$ $P_3\ P_2\ P_1\ P_0$ if (CF) = 0	Branch to the location in the same page specified by P_7 to P_0 if CF is 0.		
BZ addr	Branch on ZF	1 1 0 1 $P_7\ P_6\ P_5\ P_4$	1 1 0 1 $P_3\ P_2\ P_1\ P_0$	2	2	PC7 to 0 ← $P_7\ P_6\ P_5\ P_4$ $P_3\ P_2\ P_1\ P_0$ if (ZF) = 1	Branch to the location in the same page specified by P_7 to P_0 if ZF is 1.		
BNZ addr	Branch on no ZF	1 0 0 1 $P_7\ P_6\ P_5\ P_4$	1 1 0 1 $P_3\ P_2\ P_1\ P_0$	2	2	PC7 to 0 ← $P_7\ P_6\ P_5\ P_4$ $P_3\ P_2\ P_1\ P_0$ if (ZF) = 0	Branch to the location in the same page specified by P_7 to P_0 if ZF is 0.		
BFn4 addr	Branch on flag bit	1 1 1 1 $P_7\ P_6\ P_5\ P_4$	$n_3\ n_2\ n_1\ n_0$ $P_3\ P_2\ P_1\ P_0$	2	2	PC7 to 0 ← $P_7\ P_6\ P_5\ P_4$ $P_3\ P_2\ P_1\ P_0$ if (Fn) = 1	Branch to the location in the same page specified by P_0 to P_7 if the flag (of the 16 user flags) specified by $n_3\ n_2\ n_1\ n_0$ is 1.		
BNFn4 addr	Branch on no flag bit	1 0 1 1 $P_7\ P_6\ P_5\ P_4$	$n_3\ n_2\ n_1\ n_0$ $P_3\ P_2\ P_1\ P_0$	2	2	PC7 to 0 ← $P_7\ P_6\ P_5\ P_4$ $P_3\ P_2\ P_1\ P_0$ if (Fn) = 0	Branch to the location in the same page specified by P_0 to P_7 if the flag (of the 16 user flags) specified by $n_3\ n_2\ n_1\ n_0$ is 0.		
[I/O instructions]									
IP0	Input port 0 to AC	0 0 1 0	0 0 0 0	1	1	AC ← (P0)	Input the contents of port 0 to AC.	ZF	
IP	Input port to AC	0 0 1 0	0 1 1 0	1	1	AC ← [P (DP_L)]	Input the contents of port P (DP_L) to AC.	ZF	
IPM	Input port to M	0 0 0 1	1 0 0 1	1	1	M (HL) ← [P (DP_L)]	Input the contents of port P (DP_L) to M (HL).		
IPDR i4	Input port to AC direct	1 1 0 0 0 1 1 0	1 1 1 1 $I_3\ I_2\ I_1\ I_0$	2	2	AC ← [P (i4)]	Input the contents of P (i4) to AC.	ZF	
IP45	Input port 4, 5 to E, AC respectively	1 1 0 0 1 1 0 1	1 1 1 1 0 1 0 0	2	2	E ← [P (4)] AC ← [P (5)]	Input the contents of ports P (4) and P (5) to E and AC respectively.		
OP	Output AC to port	0 0 1 0	0 1 0 1	1	1	P (DP_L) ← (AC)	Output the contents of AC to port P (DP_L).		
OPM	Output M to port	0 0 0 1	1 0 1 0	1	1	P (DP_L) ← [M (HL)]	Output the contents of M (HL) to port P (DP_L).		
OPDR i4	Output AC to port direct	1 1 0 0 0 1 1 1	1 1 1 1 $I_3\ I_2\ I_1\ I_0$	2	2	P (i4) ← (AC)	Output the contents of AC to P (i4).		
OP45	Output E, AC to port 4, 5 respectively	1 1 0 0 1 1 0 1	1 1 1 1 0 1 0 1	2	2	P (4) ← (E) P (5) ← (AC)	Output the contents of E and AC to ports P (4) and P (5) respectively.		
SPB t2	Set port bit	0 0 0 0	1 0 $t_1\ t_0$	1	1	[P (DP_L), t2] ← 1	Set to one the bit in port P (DP_L) specified by the immediate data $t_1\ t_0$.		
RPB t2	Reset port bit	0 0 1 0	1 0 $t_1\ t_0$	1	1	[P (DP_L), t2] ← 0	Clear to zero the bit in port P (DP_L) specified by the immediate data $t_1\ t_0$.	ZF	
ANDPDR i4, p4	And port with immediate data then output	1 1 0 0 $I_3\ I_2\ I_1\ I_0$	0 1 0 1 $P_3\ P_2\ P_1\ P_0$	2	2	P (P_3 to P_0) ← [P (P_3 to P_0)] ∨ I_3 to I_0	Take the logical and of P (P_3 to P_0) and the immediate data $I_3\ I_2\ I_1\ I_0$ and output the result to P (P_3 to P_0).	ZF	
ORPDR i4, p4	Or port with immediate data then output	1 1 0 0 $I_3\ I_2\ I_1\ I_0$	0 1 0 0 $P_3\ P_2\ P_1\ P_0$	2	2	P (P_3 to P_0) ← [P (P_3 to P_0)] ∨ I_3 to I_0	Take the logical or of P (P_3 to P_0) and the immediate data $I_3\ I_2\ I_1\ I_0$ and output the result to P (P_3 to P_0).	ZF	

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Mnemonic		Instruction code		Number of bytes	Number of cycles	Operation	Description	Affected status bits	Note
		D_7 D_6 D_5 D_4	D_3 D_2 D_1 D_0						
[Timer control instructions]									
WTTM0	Write timer 0	1 1 0 0	1 0 1 0	1	2	TIMER0 ← [M2 (HL)], (AC)	Write the contents of M2 (HL), AC into the timer 0 reload register.		
WTTM1	Write timer 1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 0 0	2	2	TIMER1 ← (E), (AC)	Write the contents of E, AC into the timer 1 reload register A.		
RTIM0	Read timer 0	1 1 0 0	1 0 1 1	1	2	M2 (HL), AC ← (TIMER0)	Read out the contents of the timer 0 counter into M2 (HL), AC.		
RTIM1	Read timer 1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 0 1	2	2	E, AC ← (TIMER1)	Read out the contents of the timer 1 counter into E, AC.		
START0	Start timer 0	1 1 0 0 1 1 1 0	1 1 1 1 0 1 1 0	2	2	Start timer 0 counter	Start the timer 0 counter.		
START1	Start timer 1	1 1 0 0 1 1 1 0	1 1 1 1 0 1 1 1	2	2	Start timer 1 counter	Start the timer 1 counter.		
STOP0	Stop timer 0	1 1 0 0 1 1 1 1	1 1 1 1 0 1 1 0	2	2	Stop timer 0 counter	Stop the timer 0 counter.		
STOP1	Stop timer 1	1 1 0 0 1 1 1 1	1 1 1 1 0 1 1 1	2	2	Stop timer 1 counter	Stop the timer 1 counter.		
[Interrupt control instructions]									
MSET	Set interrupt master enable flag	1 1 0 0 0 1 0 1	1 1 0 1 0 0 0 0	2	2	MSE ← 1	Set the interrupt master enable flag to 1.		
MRESET	Reset interrupt master enable flag	1 1 0 0 1 0 0 1	1 1 0 1 0 0 0 0	2	2	MSE ← 0	Clear the interrupt master enable flag to 0.		
EIH i4	Enable interrupt high	1 1 0 0 0 1 0 1	1 1 0 1 I_3 I_2 I_1 I_0	2	2	EDIH ← (EDIH) ∨ i4	Set the interrupt enable flag to 1.		
EIL i4	Enable interrupt low	1 1 0 0 0 1 0 0	1 1 0 1 I_3 I_2 I_1 I_0	2	2	EDIL ← (EDIL) ∨ i4	Set the interrupt enable flag to 1.		
DIH i4	Disable interrupt high	1 1 0 0 1 0 0 1	1 1 0 1 I_3 I_2 I_1 I_0	2	2	EDIH ← (EDIH) ∧ $\overline{i4}$	Clear the interrupt enable flag to 0.	ZF	
DIL i4	Disable interrupt low	1 1 0 0 1 0 0 0	1 1 0 1 I_3 I_2 I_1 I_0	2	2	EDIL ← (EDIL) ∧ $\overline{i4}$	Clear the interrupt enable flag to 0.	ZF	
WTSP	Write SP	1 1 0 0 1 1 0 1	1 1 1 1 1 0 1 0	2	2	SP ← (E), (AC)	Transfer the contents of E, AC to SP.		
RSP	Read SP	1 1 0 0 1 1 0 1	1 1 1 1 1 0 1 1	2	2	E, AC ← (SP)	Transfer the contents of SP to E, AC.		
[Standby control instructions]									
HALT	HALT	1 1 0 0 1 1 0 1	1 1 1 1 1 1 1 0	2	2	HALT	Enter halt mode.		
HOLD	HOLD	1 1 0 0 1 1 0 1	1 1 1 1 1 1 1 1	2	2	HOLD	Enter hold mode.		
[Serial I/O control instructions]									
STARTS	Start serial I O	1 1 0 0 1 1 1 0	1 1 1 1 1 1 1 0	2	2	START SI O	Start SIO operation.		
WTSIO	Write serial I O	1 1 0 0 1 1 1 0	1 1 1 1 1 1 1 1	2	2	SIO ← (E), (AC)	Write the contents of E, AC to SIO.		
RSIO	Read serial I O	1 1 0 0 1 1 1 1	1 1 1 1 1 1 1 1	2	2	E, AC ← (SIO)	Read the contents of SIO into E, AC.		
[Other instructions]									
NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	Consume one machine cycle without performing any operation.		
SB i2	Select bank	1 1 0 0 1 1 0 0	1 1 1 1 0 0 I_1 I_0	2	2	PC13, PC12 ← I_1 I_0	Specify the memory bank.		Illegal instruction